Claims 14-19 were pending in the present application prior to the aforementioned amendment. By this Amendment, claims 14-19 have been amended and new claims 31-44 have been added to recite additional protection to which Applicant is entitled. Applicant submits that no issue of new matter has been set forth by this Amendment. Accordingly, claims 14-19 and 31-44 are now pending in the subject application and are believed to be in condition for allowance at least for the reasons advanced hereinbelow.

Initially, the Office Action rejects claim 14 under 35 U.S.C. §102(b) as anticipated by ***Zhang*** (U.S. Patent 5,236,850), claims 15 and 17-18 under 35 U.S.C. §103(a) as unpatentable over ***Liu et al.*** (U.S. Patent 5,147,826) in view of ***Zhang '850***, claim 16 under 35 U.S.C. §103(a) as unpatentable over ***Yamazaki et al.*** (U.S. Patent 5,773,327) in view of ***Zhang '850*** and claim 19 under 35 U.S.C. §103(a) as unpatentable over ***Yamazaki et al. '327*** in view of ***Zhang '850*** and ***Fonash et al.*** (U.S. Patent 5,275,851). By the above Amendment, claims 14-19 currently set forth subject matter which is patentably distinct over the prior art of record.

The claimed invention is directed generally to a method of manufacturing a semiconductor device. More particularly, the claimed invention is directed to method for manufacturing semiconductor device comprising a semiconductor circuit comprising the steps of forming a semiconductor film through a sputtering method on the base film, and crystallizing the semiconductor film to form a crystalline semiconductor film. In accordance with an embodiment of the claimed invention set forth at least in claims 14-19, an inert gas is used as a sputtering gas in the sputtering method, the inert gas being at least one gas selected from the group consisting of Ar, He, Ne and N.

Note that "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is

contained in the...claims." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913 (Fed. Cir. 1989).

Referring now to the prior art of record, it is contended that the ***Zhang '850*** patent fails to expressly or inherently describe each and every element as set forth in claim 14 as presently amended. For instance, claim 14 now recites method steps of forming a base film on a plastic substrate and forming a semiconductor film through a sputtering method on the base film. Consequently, the substrate is inherently flexible due to it being composed of plastic, and thus, the semiconductor device formed over the plastic substrate can be used in various apparatuses such as portable devices. Such a feature is not expressly taught or implicitly described in the patent.

Accordingly, since the ***Zhang '850*** patent fails to expressly teach or inherently desribe every claim limitation necessary to support anticipation under §102, it is respectfully requested that the rejection be reconsidered and withdrawn.

Referring now to the §103 rejection, note that three criteria must be met to establish a *prima facie* case of obviousness. *M.P.E.P.* §2143. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings to achieve the claimed invention. *Id.* Second, there must be a reasonable expectation of success. *In re Rhinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976). Third, the prior art must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Applicant respectfully contends that the ***Liu et al. '826***, ***Zhang '850***, ***Yamazaki et al. '327***, and ***Fonash et al. '851*** patents, alone or in any combination thereof, fail to expressly teach or suggest all of the limitations presently set forth in the claimed invention necessary to support a *prima facie* case of obviousness under §103. Nor is there motivation in the prior art of record to either modify the respective base references

or combine the respective teachings of the prior art of record in a manner sufficient to achieve the claimed invention. For instance, claims 15 and 18 currently recite a step of crystallizing the semiconductor film by irradiating laser light. The ***Yamazaki et al. '327*** patent discloses that the crystallinity of the semiconductor region is improved by irradiating with laser beams (Col. 5, lines 52-56). However, before the step of laser irradiation, an amorphous semiconductor film is crystallized by heating at a temperature of 350-450°C for 0.1-2 hours (Col. 5, lines 63-67). The other prior art references fail to disclose the use of a laser to crystallize the semiconductor film.

As in amended claim 14, claim 17 presently recites method steps of forming a base film on a plastic substrate and forming a semiconductor film through a sputtering method. Consequently, the substrate is inherently flexible due to it being composed of plastic, and thus, the semiconductor device formed over the plastic substrate can be used in various apparatuses such as portable devices. In addition, claim 17 sets forth that Such a feature is not expressly taught or implicitly described in the proposed ***Liu et al. '826*** or ***Zhang '850*** combination.

Claim 16 presently recites a step forming an amorphous semiconductor film comprising silicon and germanium through a sputtering method on an insulating surface, this feature being described at least on page 4, line 27 through page 5, line 3 of the specification. Such a feature is not expressly taught or inherently suggested in either of the proposed ***Yamazaki et al. '327*** and ***Zhang '850*** combination.

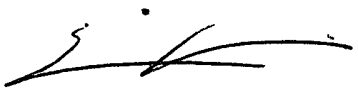
Claims 17 and 18 further recite steps of forming a gate wiring on a base film and forming a gate insulating film on the gate wiring, and forming a semiconductor film through a sputtering method on the gate insulating film, to thereby form a bottom gate device. On the other hand, each of the prior art references of record, notably the proposed ***Liu et al. '826*** or ***Zhang '850*** combination, are directed to top gate transistors.

Accordingly, since the proposed prior art modifications fail to expressly teach or suggest all of the limitations set forth in claimed invention necessary to support a *prima facie* case of obviousness under §103, it is respectfully requested that each rejection be reconsidered and withdrawn.

For at least the foregoing reasons, it is respectively asserted that claims 14-44 are in proper condition for allowance. Reconsideration of these claims in view of the above comments is respectively requested. If the Examiner feels that any further discussions would be beneficial in this matter, it is requested that the undersigned be contacted.

Respectfully submitted,

NIXON PEABODY LLP

By: 

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Marked-up copy of amended claims.

14. (Amended) A method for manufacturing semiconductor device comprising a semiconductor circuit, said method comprising the steps of:

forming a base film on a plastic substrate;

forming a semiconductor film through a sputtering method on [an insulating surface] the base film; and

crystallizing the semiconductor film to form a crystalline semiconductor film,

wherein an inert gas is used as a sputtering gas in the sputtering method, said inert gas being at least one gas selected from the group consisting of Ar, He, Ne and N.

15. (Amended) A method for manufacturing a semiconductor device comprising a semiconductor circuit, said method comprising the steps of:

forming a semiconductor film through a sputtering method on an insulating surface;

adding a catalytic element into at least a portion of the semiconductor film, said catalytic element being capable of promoting crystallization; and

crystallizing [said] the semiconductor film by irradiating with a laser light to form a crystalline semiconductor film,

wherein an inert gas is used as a sputtering gas in the sputtering method, said inert gas being at least one gas selected from the group consisting of Ar, He, Ne and N.

16. (Amended) A method for manufacturing a semiconductor device comprising a semiconductor circuit, said method comprising the steps of:

forming [a] an amorphous semiconductor film comprising silicon and germanium through a sputtering method on an insulating surface;

adding a catalytic element into at least a portion of the semiconductor film,

said catalytic element being capable of promoting crystallization;

crystallizing [said] the semiconductor film to form a crystalline semiconductor film,

[; and]

[reducing a concentration of the catalytic element in the crystalline semiconductor film]

wherein an inert gas is used as a sputtering gas in the sputtering method, said inert gas being at least one gas selected from the group consisting of Ar, He, Ne and N.

17. (Amended) A method for manufacturing a semiconductor device comprising a semiconductor circuit, said method comprising the steps of:

forming a base film on a plastic substrate;

forming a gate wiring on the base film;

forming a gate insulating film on the gate wiring;

forming a semiconductor film through a sputtering method on [an] the gate insulating [surface] film;

[forming an insulating film being in contact with the semiconductor film; and]

crystallizing [said] the semiconductor film [while being in contact with the insulating film] to form a crystalline semiconductor film,

wherein an inert gas is used as a sputtering gas in the sputtering method, said inert gas being at least one gas selected from the group consisting of Ar, He, Ne and N.

18. (Amended) A method for manufacturing a semiconductor device comprising a semiconductor circuit, said method comprising the steps of:

forming a gate wiring an insulating surface;

forming a gate insulating film on the gate wiring;

[adding a catalytic element into at least a portion of an insulating surface, said catalytic element being capable of promoting crystallization;]

forming a semiconductor film through a sputtering method on the gate insulating film;

[forming an insulating film being in contact with the semiconductor film; and]

crystallizing [said] the semiconductor film [while being in contact with the insulating film] by irradiating with a laser light to form a crystalline semiconductor film,

wherein an inert gas is used as a sputtering gas in the sputtering method, said inert gas being at least one gas selected from the group consisting of Ar, He, Ne and N.

19. (Amended) A method for manufacturing [a semiconductor] an electroluminescence display device comprising at least a thin film transistor [a semiconductor circuit], said method comprising the steps of:

[adding a catalytic element into at least a portion of an insulating surface, said catalytic element being capable of promoting crystallization;]

forming a semiconductor film through a sputtering method on an insulating surface;

[forming an insulating film being in contact with the semiconductor film;]

crystallizing [said] the semiconductor film [while being contact with the insulating film] to form a crystalline semiconductor film; [and]

[reducing a concentration of the catalytic element in the crystalline semiconductor film]

forming a gate insulating film adjacent to the crystalline semiconductor film;

forming a gate electrode adjacent to the crystalline semiconductor film with the gate insulating film interposed therebetween;

introducing an impurity region into the crystalline semiconductor film to form at least a source region, a drain region and a channel region between the source and drain regions;

forming at least an interlayer insulating film over the thin film transistor;

forming a pixel electrode over the interlayer insulating film, said pixel electrode being electrically connected to the drain region of the thin film transistor;

forming an EL layer adjacent to the pixel electrode;

forming a cathode adjacent to the EL layer,

wherein an inert gas is used as a sputtering gas in the sputtering method, said inert gas being at least one gas selected from the group consisting of Ar, He, Ne and N.